REMARKS/ARGUMENTS

The non-final office action of March 13, 2006, has been carefully reviewed and these remarks are responsive thereto. Claims 7, 18, 22, and 25 have been amended. Claim 21 has been canceled without prejudice or disclaimer. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-20 and 22-25 remain pending.

Claims 18-22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Cote et al. (U.S. Patent No. 6,470,485, hereinafter referred to as *Cote*). Applicants respectfully traverse the rejection.

Applicants have amended claim 18 to include many of the features of original dependent claim 21. As amended, Applicants' claim 18 recites, among other features, "wherein the first set is further configured to provide an *N*-bit input generator to the second set and to provide a configurable logic block, separate from the *N*-bit input generator, as a verifier to verify the output data of the second set." In rejecting this feature of original dependent claim 21, the Action relies on Figure 3C and column 25, lines 6-26 of *Cote*. Neither the cited portion nor any other portion of *Cote* teaches such a feature.

In order establish a prima facie case of anticipation under 35 U.S.C. § 102(e), each and every feature of the claim must be taught by the reference. *Cote* describes a method and structures for testing a configurable interconnect network in an FPGA device. (*Abstract, Title*). The cited portion of *Cote* describes how multiple Variable Grain Block (VGB) structures may be used for a feedback loop of an FPGA-implemented sequencer. (Col. 25, ll. 6-11). The five output registers of a fist VGB_A is connected to the five input decoder of a second VGB_M and the five output registers of the second VGB_M is connected to the five input decoder of the first VGB_A. (Figure 3C). *Cote* fails to describe an *N*-bit input generator and a separate verifier configurable logic block. The registers in a first VGB of *Cote* act as the inputs to a second VGB and the same registers store current state bits. Even assuming without admitting that the registers in *Cote* are an *N*-bit input generator, the same registers would have to act as the verifier. As such, even assuming without admitting that *Cote* describes such a configuration, the *N*-bit input generator is not separate from the verifier configurable logic block. As *Cote* fails to teach or

suggest every feature of Applicants' amended claim 18, withdrawal of the present rejection is respectfully requested.

Claims 19-20, 22, which depend from claim 18, are allowable over the art of record for all the reasons given above concerning their respective base claim, and further in view of the novel features recited therein. For example, Applicants' claim 22 recites, "wherein an output of the verifier is an input to the verifier, and wherein the output of the verifier is a failure indicator." No portion of *Cote* teaches or suggests at least this feature of Applicants' claim 22.

Claims 1-6 and 9-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Farooq (U.S. Patent No. 6,760,277, hereinafter referred to as *Farooq*) in view of Herron et al. (U.S. Patent No. 6,996,758, hereinafter referred to as *Herron*). Claims 7-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Farooq* in view of *Herron* and further in view of Myers (U.S. Patent No. 5,278,841, hereinafter referred to as *Myers*). Applicants respectfully traverse the rejections.

In order to establish a *prima facie* case of obviousness under § 103(a), three criteria must exist: 1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings; 2) there must be a reasonable expectation of success; and 3) the prior art reference(s) must teach or suggest all the claim limitations. *See* MPEP § 706.02 (j); *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991).

Even assuming, without admitting, that the combination of *Farooq* and *Herron* does teach or suggest each and every feature of Applicants' claim 1, there is no proper motivation for combining the two references. The Federal Circuit has repeatedly stated that the limitations of a claim in a pending application cannot be used as a blueprint to piece together prior art in hindsight, *In re Dembiczak*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999), and that the Patent Office should *rigorously* apply the requirement that a teaching or motivation to combine prior art references needs to be provided. *Id.* (emphasis added). Applicants contend that there is no motivation or suggestion to combine *Farooq* with *Herron*.

The Action provides its motivation to combine stating, "[t]his modification would have been obvious to one of ordinary skill in the art, at the time invention was made, because one of ordinary skill in the art would have recognized that configuring a first set of configurable logic blocks to be first testing circuitry would provide the opportunity to configure the logic blocks to test other parts of the system.." (Action, page 4). This is not a motivation to combine references, but is a conclusion that has apparently been reached after having benefited from reading Applicants' own disclosure, and is thus impermissible hindsight.

Although *Farooq* and *Herron* describe FPGAs, both fail to provide a motivation to combine its teachings with those of the other. Applicants respectfully submit that that there is no motivation or suggestion to combine *Farooq* with *Herron*. Even assuming that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning, the Action provides no evidence that the combination takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, nor does the Action provide any evidence that the combination includes knowledge other than that gleaned from Applicants' disclosure. Thus, the combination is improper based on hindsight. As the Action fails to cite any portion of *Farooq* or *Herron* for the motivation to combine the references, Applicants respectfully request withdrawal of the present rejection.

With respect to the rejection of claims 7 and 8, the Action again fails to cite any portion of *Farooq*, *Herron*, or *Myers* as evidence of the motivation to combine the references. The Action merely states, "[t]his modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide N-bit input to the second set of configurable logic blocks." Again, such a statement is nothing more that a blanket comment without any support in any of the references. The Action merely attempts to piece together various references to reject the claim without any cited evidence of motivation to combine the references together.

Applicants' claims 2-12, which depend on claim 1, are patentably distinct over the art of record for at least the same reasons as their ultimate base claim and further in view of the novel features recited therein. For example, Applicants' claim 3 recites, among other features,

"configuring a third set of configurable logic blocks to be second testing circuitry; and operating the third set, concurrently with the first set, to test a fourth set of configurable logic blocks." The combination of *Farooq* and *Herron*, even if proper, fails to teach or suggest at least this feature. In particular, the combination of references fails to teach concurrent operation of sets to test another set. Applicants' claim 7 recites, among other features, "wherein the step of configuring the $N \geq 1$ configurable logic blocks includes configuring the $N \geq 1$ configurable logic blocks to operate as an *N*-bit counter." *Myers* fails to teach or suggest that the three-bit binary counter 43 is made up of configurable logic blocks. Counter 43 in *Myers* is never described more than a traditional binary counter.

Claims 13-17 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Butts et al. (U.S. Patent No. 5,036,473, hereinafter referred to as *Butts*) in view of *Cote*. Applicants respectfully traverse the rejection.

Even assuming, without admitting, that the combination of *Butts* and *Cote* does teach or suggest each and every feature of Applicants' claim 13, there is no proper motivation for combining the two references. The Action fails to provide any evidence in the references for motivation to combine them and merely provides its motivation to combine by stating, "[t]his modification would have been obvious to one of ordinary skill in the art, at the time invention was made, because one of ordinary skill in the art would have recognized that using the method of testing routing portions in an emulation system would provide the opportunity to verify all parts of the interconnect within the IC correctly and consistently route all signals in timely and accurate fashion between configurable logic blocks." (Action, page 7). Again, this is not a motivation to combine references, but is a conclusion that has apparently been reached after having benefited from reading Applicants' own disclosure, and is thus impermissible hindsight.

Even assuming that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning, the Action provides no evidence that the combination takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, nor does the Action provide any evidence that the combination includes knowledge other than that gleaned from Applicants' disclosure. Thus, the combination is improper based on hindsight. As the Action fails to cite any portion of *Butts* or

Cote for the motivation to combine the references, Applicants respectfully request withdrawal of the present rejection.

In addition, even assuming, without admitting, that the combination of *Butts* and *Cote* is proper, the combination fails to teach or suggest each and every feature of Applicants' claim 13. Applicants' claim 13 recites, among other features, "configuring a second routing portion to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second configuration inverse to the first configuration." Butts describes channel routing interconnects used to route outputs form one logic chip to inputs of another logic chip; however, *Butts* does not describe the above noted feature of Applicants' claim 13. In particular, *Butts* does not explicitly describe that the second configuration is inverse to the first configuration. Cote fails to teach or suggest such a feature as well. As such, the combination of references fails to teach or suggest each and every feature of Applicants' claim 13 and withdrawal of the rejection is respectfully requested.

Applicants' claims 14-17, which depend on claim 13, are patentably distinct over the art of record for at least the same reasons as their ultimate base claim and further in view of the novel features recited therein.

With respect to claim 23, the Action fails to provide any motivation in either reference to combine the two references (Action, page 8). As such, the motivation to combine the two references for rejection of claim 23 is improper. In addition, Applicants' claim 23 includes similar features as described above with reference to claim 13. As such, Applicants' claim 13 is patentably distinct over the art of record for at least similar reasons as described with respect to claim 13.

Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tseung et al. (U.S. Patent No. 5,903,744, hereinafter referred to as *Tseung*) in view of *Cote*. Applicants respectfully traverse the rejection.

Even assuming, without admitting, that the combination of *Tseung* and *Cote* does teach or suggest each and every feature of Applicants' claim 24, there is no proper motivation for combining the two references. The Action fails to provide any evidence in the references for motivation to combine them and merely provides its motivation to combine by stating, "[t]his

modification would have been obvious to one of ordinary skill in the art, at the time invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify interconnect boards including integrated circuits so that the signals can be routed correctly." (Action, page 9). Again, this is not a motivation to combine references, but is a conclusion that has apparently been reached after having benefited from reading Applicants' own disclosure, and is thus impermissible hindsight.

Even assuming that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning, the Action provides no evidence that the combination takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, nor does the Action provide any evidence that the combination includes knowledge other than that gleaned from Applicants' disclosure. Thus, the combination is improper based on hindsight. As the Action fails to cite any portion of *Tseung* or *Cote* for the motivation to combine the references, Applicants respectfully request withdrawal of the present rejection.

In addition, even assuming, without admitting, that the combination of *Tseung* and *Cote* is proper, the combination fails to teach or suggest each and every feature of Applicants' claim 24. Applicants' claim 24 recites, among other features, "wherein the data processing portion is configured to provide a first test pattern to the first set to test the second set and a second test pattern to the second set to test the first set." As admitted by the Action, *Tseung* fails to teach such a feature. (Action, page 9). In rejecting this feature, the Action relies on various portions of *Cote*. However, no portion of *Cote* teaches or suggests such a feature. As described in *Cote*, "[o]ne of the application programs 465 may be an FPGA configuring and testing program structured to cause the FPGA to self-test itself in accordance with the invention described herein." (Col. 27, ll. 18-21). Under *Cote*, the system would utilize a first test pattern to self-test and not to test a different set. As such, the combination of *Tseung* and *Cote* fails to teach or suggest each and every feature of Applicants' claim 24 and withdrawal of the present rejection is respectfully requested.

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tseung* in view of *Butts* and further in view of *Cote*. Applicants respectfully traverse the rejection.

As with each of the other claims rejected under 35 U.S.C. § 103(a), the Action fails to cite any portion of the references and/or provide any evidence to support the motivation to combine the references. Again, the combination is improper based on hindsight. As the Action fails to cite any portion of *Tseung*, *Butts*, or *Cote* for the motivation to combine the references, Applicants respectfully request withdrawal of the present rejection. In addition, the combination of references, even if proper, fails to teach or suggest each and every feature of amended claim 25. In particular, none of the references teaches or suggests the claim 25 feature of, "wherein the second routing portion is configured to map *N* inputs of the second routing portion to *N* outputs of the second routing portion in a second manner inverse to the first manner." Therefore, for at least these reasons, withdrawal of the rejection of amended claim 25 is respectfully requested.

CONCLUSION

All rejections having been addressed, Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same. However, if for any reason the Examiner believes the application is not in condition for allowance or there are any questions, the examiner is requested to contact the undersigned at (202) 824-3155.

Respectfully submitted,
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